

FIG. 1a is a schematic diagram of a device 100. The device 100 includes a substrate 4, a layer 6, and a layer 8. The layer 6 is disposed on the substrate 4, and the layer 8 is disposed on the layer 6. The layer 8 includes a pattern 2.

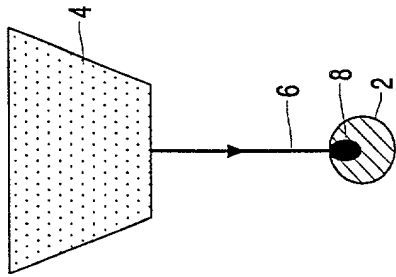


FIG. 1a

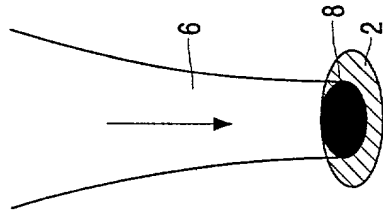


FIG. 1b

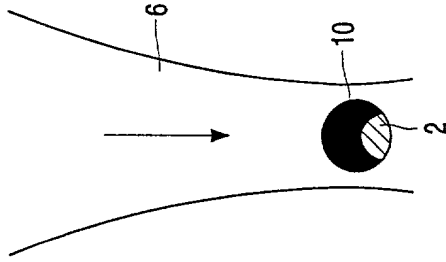


FIG. 1c

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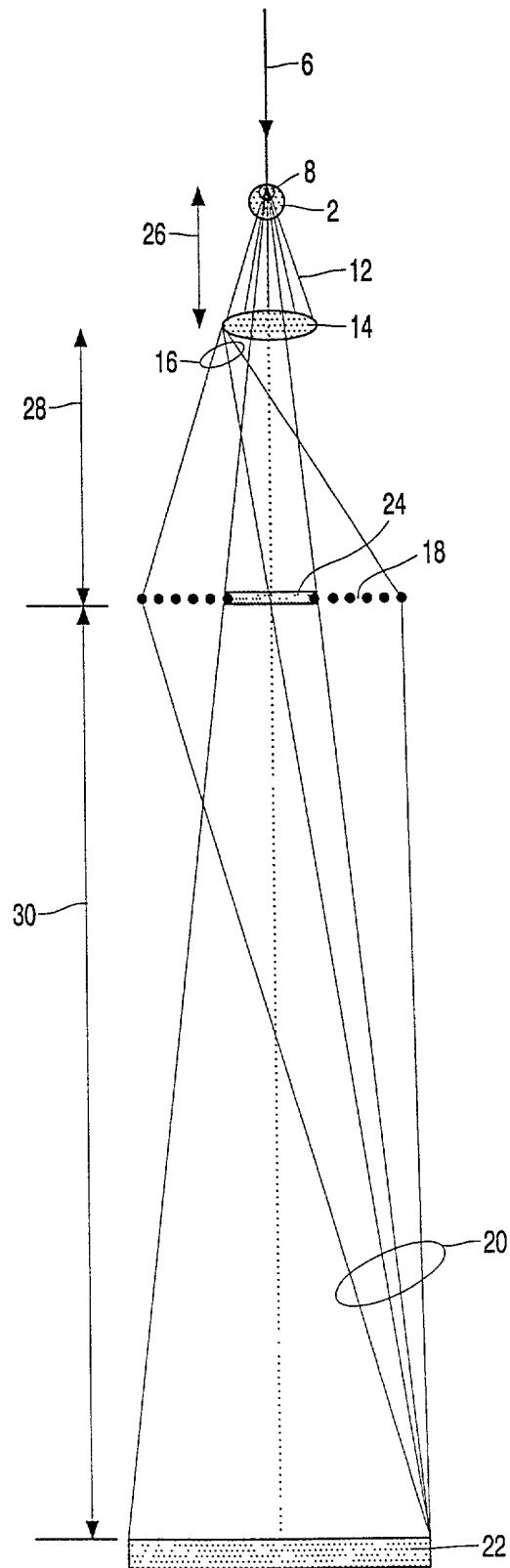


FIG. 2

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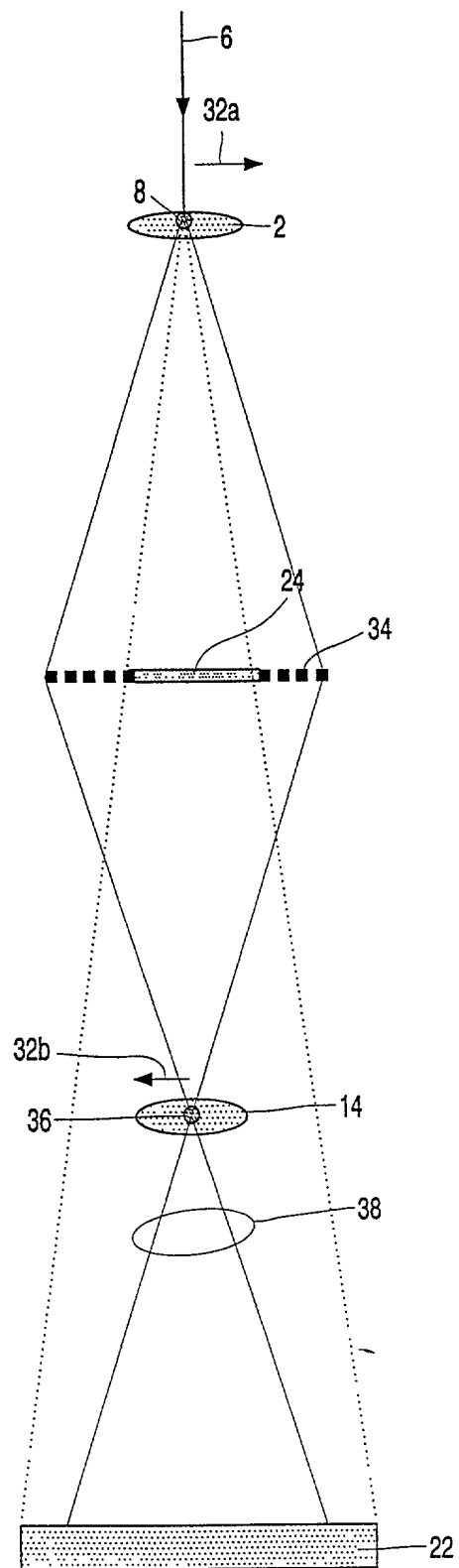


FIG. 3

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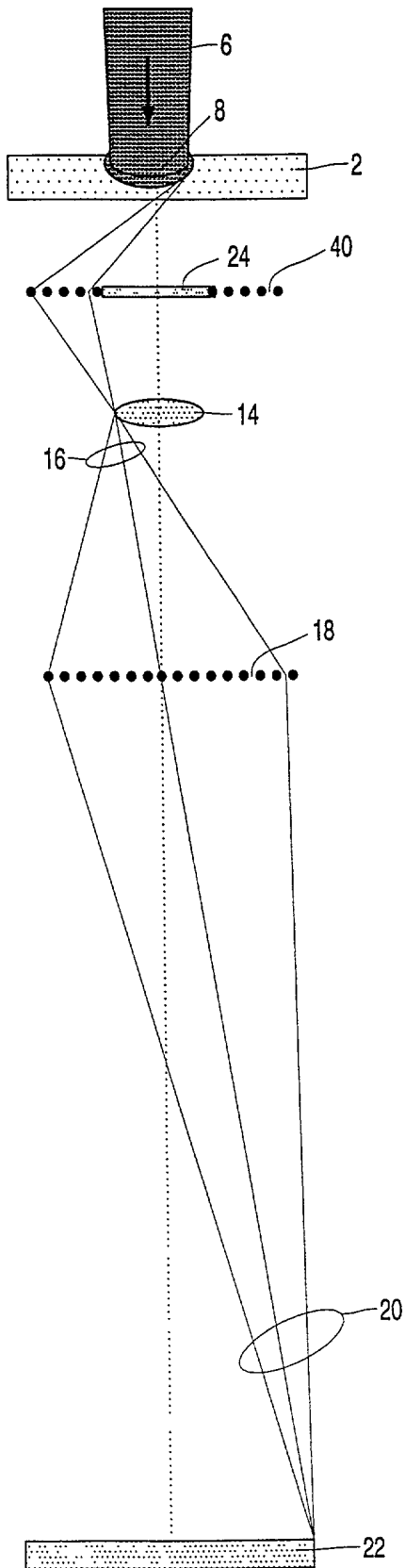


FIG. 4